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# Analytical Method to Calculate the DC Link Current Stress in Voltage Source Converters

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**Abstract**—The dc-link capacitor is one of the critical components, which influences the lifetime of the whole voltage source converter unit. For reliable design, the operating temperature of the dc-link capacitor should be known, which is primarily determined by the ambient temperature and the rms value of the current flowing through the dc-link capacitor. A simple analytical method to calculate the rms value of the dc-link capacitor current is presented in this paper. The effect of the line current ripple on the rms value of the dc-link capacitor current is considered. This yields accurate results, especially for the applications with high line current ripple. The effect of the pulsewidth modulation (PWM) scheme on the rms value of the dc-link current is also studied and the analysis for continuous PWM and discontinuous PWM (DPWM) schemes is presented. The proposed analytical method is also verified experimentally.

## I. INTRODUCTION

Three-phase Pulsewidth Modulated (PWM) Voltage Source Converter (VSC) is widely used as a dc/ac converter in many power electronics applications and the dc-link capacitor is generally employed to balance the instantaneous power difference between the input and output [1], [2]. The design of the dc-link capacitor needs careful attention, as it is one of the critical components which influences the lifetime of the whole system [3]. The predicted lifetime of the capacitor, considering the effect of temperature rise, is given using the empirical lifetime model [1] as

$$L_p = L_r \left( \frac{V}{V_r} \right)^{-n} e^{\left[ \left( \frac{E_a}{K_B} \right) \left( \frac{1}{T} - \frac{1}{T_r} \right) \right]} \quad (1)$$

where  $L_p$  and  $L_r$  are the predicted and rated lifetimes of the capacitor, respectively.  $V$  and  $V_r$  are the voltages at the use condition and rated condition, respectively.  $E_a$  is the activation energy and  $K_B$  is the Boltzmann's constant.  $T_r$  is the rated temperature, whereas  $T$  is the temperature at the operating condition. A simplified lifetime model can be derived from (1), and it is given as

$$L_p = L_r 2^{\left( \frac{T_r - T}{10} \right)} \quad (2)$$

From (2), it can be seen that the lifetime of the capacitor can be improved by keeping the  $T$  below the rated temperature  $T_r$  [4]. For the given capacitor and the ambient temperature, the temperature rise of the capacitor is mainly determined by the rms value of the current flowing through it. Thus, the accurate estimation of the dc-link rms current is inevitable for reliable design of the system.

The rms value of the dc-link capacitor current is calculated using the time domain approach in [2], [5]. Only the fundamental component of the line current is considered for synthesizing the dc-link current and the effect of line current ripple is neglected. This leads to the larger relative error in certain operating conditions [2]. Also, different PWM schemes exhibit distinct line current ripple [6], and by neglecting the effect of the line current ripple, it is not possible to evaluate the effect of the PWM scheme on the rms value of dc-link capacitor current [7]. Another approach is to evaluate the harmonic spectrum of the dc-link current in frequency domain using double Fourier series [7]–[9]. However this method is more computational intensive compared to the first approach [7].

A simple analytical method to calculate the rms value of the dc-link current using time domain approach is presented in this paper. The ripple component of the line current is also considered for synthesizing the dc-link current. Thus accurate results are obtained and the influence of the PWM scheme on the dc-link current stress can also be analyzed. The rms value of the dc-link current for center aligned Space Vector Modulation (SVM) and the DPWM1 (60° clamp) [10] is evaluated. The effect of the modulation index  $M$  and the displacement power factor angle on the rms value of the dc-link current is also analyzed.

The paper is organized as follows. The system considered for the study is described in Section II. The proposed analytical method for calculating the rms value of the dc-link current is presented in Section III. The influence of the various operating conditions and the PWM scheme on the dc-link current stress is analyzed in Section IV. The proposed analytical method is verified experimentally and the results are presented in Section V.

## II. SYSTEM OVERVIEW

A two level three phase VSC is shown in Fig. 1. The VSC is connected to the grid through a line filter inductor  $L_f$ . The capacitor current can be given as

$$I_{cap} = I - I_{dc} \quad (3)$$

where  $I$  is the input current of the VSC and  $I_{dc}$  is the current supplied by the source. Depending on the application, the  $I_{dc}$  can be directly obtained from the battery as in the case of electric vehicle or from the mains through an input stage converter. The ripple component in the  $I_{dc}$  is assumed to be

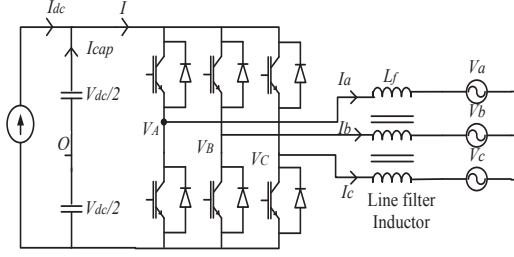


Fig. 1. System schematic of a voltage source converter with L-filter

zero for simplicity. Assuming a loss-less system, the power balance equation in steady-state gives

$$P_{dc} = P_{ac} \quad (4)$$

where  $P_{dc}$  is the power supplied by the source and  $P_{ac}$  is the active component of the power delivered by the VSC, and it is given as

$$\begin{aligned} P_{dc} &= V_{dc} I_{dc} \\ P_{ac} &= \frac{3}{2} V_D I_D \end{aligned} \quad (5)$$

where  $V_{dc}$  is the dc-link voltage,  $V_D$  and  $I_D$  are the dc values of the  $d$ -axis component of the output voltage and the line current, respectively in the synchronously rotating frame at the fundamental frequency. Using (4) and (5), the dc component of the current drawn from the source is given as

$$I_{dc} = \frac{3V_D I_D}{2V_{dc}} \quad (6)$$

In addition to  $I_{dc}$ ,  $I$  is also required in order to obtain  $I_{cap}$ , and it is given as

$$I = S_a I_a + S_b I_b + S_c I_c \quad (7)$$

where  $I_a$ ,  $I_b$ , and  $I_c$  are the line currents of phase A, phase B, and phase C, respectively and  $S_a$ ,  $S_b$  and  $S_c$  are the logic-type switching function [10], used to express the ON/OFF state of the switch. This switching function is given as

$$S_x = \begin{cases} 1, & \text{if top switch is ON} \\ 0, & \text{if bottom switch is ON} \end{cases} \quad (8)$$

where  $x$  is the corresponding phase ( $x = \{A, B, C\}$ ).

### III. DC-LINK CURRENT STRESS CALCULATION

The reference space vector  $\vec{V}_{ref}$  is synthesized using active and zero voltage vectors and the volt-second balance is maintained by choosing appropriate dwell time of these vectors. The dwell time of each voltage vector is given as

$$T_1 = \frac{\sqrt{3}}{2} M T_s \sin(60^\circ - \psi) \quad (9a)$$

$$T_2 = \frac{\sqrt{3}}{2} M T_s \sin(\psi) \quad (9b)$$

$$T_z = T_s - T_1 - T_2 \quad (9c)$$

where  $\psi$  is the angle of the reference space vector and  $M$  is the modulation index, defined as the ratio of the amplitude of

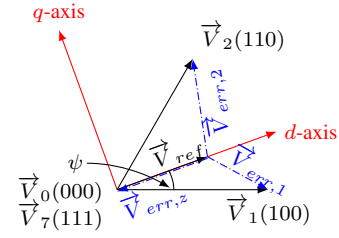


Fig. 2. The active and zero vectors to synthesize given reference vector and corresponding error voltage vectors.

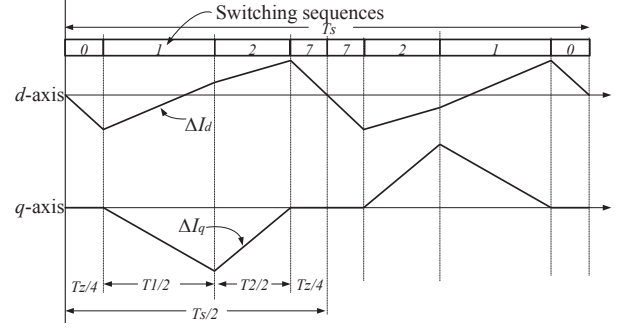


Fig. 3. The  $d$ -axis and  $q$ -axis ripple current components of the line current for the SVM. The modulation index  $M=0.85$  and reference space vector angle  $\psi=23^\circ$ .

the fundamental component of the phase voltage to the half of the dc-link voltage.

The application of the discrete vectors results in an error between the applied voltage vector and the reference voltage vector as shown in Fig. 2. The time integral of the error voltage vector is known as the harmonic flux vector [6], [11]–[13], which is directly proportional to the ripple current, and it is used in this paper to calculate the line current ripple. In the reference frame, rotating synchronously at the fundamental frequency, the instantaneous error voltage vectors can be decomposed into  $d$ -axis and the  $q$ -axis components and given as

$$\begin{aligned} \vec{V}_{err,1} &= \frac{2}{3} V_{dc} \left\{ \left( \cos \psi - \frac{3}{4} M \right) - j \sin \psi \right\} \\ \vec{V}_{err,2} &= \frac{2}{3} V_{dc} \left\{ \left[ \cos(60^\circ - \psi) - \frac{3}{4} M \right] + j \sin(60^\circ - \psi) \right\} \\ \vec{V}_{err,z} &= -\frac{1}{2} V_{dc} M \end{aligned} \quad (10)$$

Using (10), the  $d$ -axis ( $\Delta I_d$ ) and the  $q$ -axis ( $\Delta I_q$ ) ripple components in the line current are obtained, and it is depicted in Fig. 3 for the SVM. The fundamental component of the line current appears as a dc component in the frame, rotating synchronously at the fundamental frequency. The dc components of both  $d$ -axis and  $q$ -axis ( $I_D$ ,  $I_Q$ ) current are assumed to be constant during each sampling interval. Therefore, the  $d$ -axis

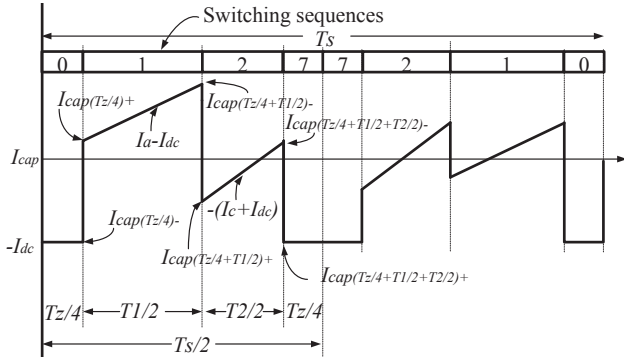


Fig. 4. Capacitor current waveform in a switching cycle.

and  $q$ -axis current in the rotating reference frame is given as

$$I_d = I_D + \Delta I_d \quad (11)$$

$$I_q = I_Q + \Delta I_q \quad (12)$$

The dc components of both  $d$ -axis and  $q$ -axis current are given as

$$I_D = I_m \cos \phi \quad (13)$$

$$I_Q = I_m \sin \phi \quad (14)$$

where  $I_m$  is the peak value of the fundamental component of the line current and the  $\phi$  is the displacement power factor angle. The line currents can be obtained from the  $d$ -axis and  $q$ -axis currents ( $I_d$ ,  $I_q$ ) using the frame transformation. For a three phase three line system, which is considered in this paper, the line currents of only two phases are required to obtain  $I_{cap}$  and it is given as

$$I_a = I_d \cos \psi - I_q \sin \psi \quad (15a)$$

$$I_c = I_d \cos(\psi + 120^\circ) - I_q \sin(\psi + 120^\circ) \quad (15b)$$

The VSC input current and thus the dc-link capacitor current can be obtained by using (3) and (7). The dc-link capacitor current can be represented by a piece-wise linear equation and rms value can be easily calculated. This is illustrated in the following sub-section for the switching sequence "0127", where the switching sequence represents the order in which the voltage vectors are applied in a switching cycle.

#### A. RMS Current Calculation

The switching sequences used in the SVM is shown in Fig. 4. The analysis is presented for the asymmetrical regularly sampled PWM, where the magnitude of the reference space vector  $|\vec{V}_{ref}|$  and the reference space vector angle  $\psi$  are sampled in each half of the switching period. For the SVM, switching sequence "0127" is used first half of the switching period, whereas the switching sequence "7210" is used in another half. The analysis for the "0127" is presented, however the results for other switching sequences are also summarized. The capacitor current is symmetrical in each sector of the space vector and thus the rms calculation in one sector ( $0 \leq \psi < 60^\circ$ ) is sufficient.

- 1) Mode 1 ( $0_+ \leq t \leq (\frac{T_z}{4})_-$ ): During this interval voltage vector  $\vec{V}_0$  is applied for the  $T_z/4$  duration. All bottom switches of the legs are turned on. For the three phase three wire system, the VSC input current  $I$  is zero during this interval. Using (3), the capacitor current is given as

$$I_{cap}(t) = -I_{dc} \quad (16)$$

and the mean square value for this interval is given as

$$F_1^2 = \frac{T_z}{2T_s} I_{dc}^2 \quad (17)$$

- 2) Mode 2 ( $(\frac{T_z}{4})_+ \leq t \leq (\frac{T_z}{4} + \frac{T_1}{2})_-$ ): Voltage vector  $\vec{V}_1$  is applied for the  $T_1/2$  duration. During this interval, phase A is clamped to the positive dc-link, whereas phase B and phase C are clamped to negative dc-link. Thus, the VSC input current  $I$  is completely characterized by the line current of phase A. The capacitor current during this interval is represented as

$$I_{cap}(t) = \left[ (I_D \cos \psi - I_Q \sin \psi) - \frac{V_{dc} T_z}{6L_f} - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 - \frac{3}{4} M \cos \psi \right) t \quad (18)$$

The mean square value in mode 2 is given as

$$F_2^2 = \frac{T_1}{3T_s} \left[ (I_{cap}(\frac{T_z}{4})_+)^2 + (I_{cap}(\frac{T_z}{4} + \frac{T_1}{2})_-)^2 + (I_{cap}(\frac{T_z}{4})_+ \times I_{cap}(\frac{T_z}{4} + \frac{T_1}{2})_-) \right] \quad (19)$$

- 3) Mode 3 ( $(\frac{T_z}{4} + \frac{T_1}{2})_+ \leq t \leq (\frac{T_z}{4} + \frac{T_1}{2} + \frac{T_2}{2})_-$ ): Due to the application of voltage vector  $\vec{V}_2$  during this interval, the VSC input current  $I$  is equal to the negative value of the line current of phase C. The capacitor current in this interval is given as

$$I_{cap}(t) = \left[ (I_Q \sin(\psi + 120^\circ) - I_D \cos(\psi + 120^\circ)) - \frac{V_{dc}(T_z + T_1)}{6L_f} - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 + \frac{3}{4} M \cos(\psi + 120^\circ) \right) t \quad (20)$$

The mean square value in mode 3 is given as

$$F_3^2 = \frac{T_2}{3T_s} \left[ (I_{cap}(\frac{T_z}{4} + \frac{T_1}{2})_+)^2 + (I_{cap}(\frac{T_z}{4} + \frac{T_1}{2} + \frac{T_2}{2})_-)^2 + (I_{cap}(\frac{T_z}{4} + \frac{T_1}{2})_+ \times I_{cap}(\frac{T_z}{4} + \frac{T_1}{2} + \frac{T_2}{2})_-) \right] \quad (21)$$

- 4) Mode 4 ( $(\frac{T_z}{4} + \frac{T_1}{2} + \frac{T_2}{2})_+ \leq t \leq (\frac{T_s}{2})_-$ ): The VSC input current  $I$  is zero due to the application of the zero voltage vector  $\vec{V}_7$ , during this interval and thus, the capacitor current is given as

$$I_{cap}(t) = -I_{dc} \quad (22)$$

which is same as the capacitor current in mode 1. Therefore, the  $F_1 = F_3$ .

The rms value of the capacitor current for the  $k^{th}$  sampling interval is then given as

$$I_{cap(rms),k} = \sqrt{F_{1k}^2 + F_{2k}^2 + F_{3k}^2 + F_{4k}^2} \quad (23)$$

The use of different switching sequences results in distinct ripple current behavior in the line current. Also different PWM schemes are using different combination of these switching sequences. The piece-wise linear equations, describing the dc-link capacitor current for different sequences are given in Table. I.

The SVM uses switching sequences "0127" in one half of the switching period and "7210" in the other half of the switching period and using them, the average of the rms value of the dc-link current over a sector ( $0 \leq \psi < 60^\circ$ ) can be calculated using

$$I_{cap(rms)} = \frac{3f_0}{f_{sw}} \sum_{k=1}^{\left(\frac{f_{sw}}{3f_0}\right)} I_{cap(rms),k} \quad (24)$$

where  $f_0$  is the fundamental frequency and  $f_{sw}$  is the switching frequency.

#### IV. ANALYSIS OF THE DC-LINK CURRENT STRESS

The dc-link capacitor current strongly depends on the modulation index  $M$ , the displacement power factor angle, and the PWM scheme used. The effect of these factors on the dc-link capacitor current are analyzed in this section.

##### A. The Effect of the Modulation Index and the Reference Space Vector Angle $\psi$

For the given modulation index, the dwell time of the voltage vectors changes with the change in the space vector angle  $\psi$  and thus the rms value of the dc-link capacitor current also varies. Fig. 5. shows the variation in the  $I_{cap(rms)}$  for the SVM with the  $\psi$  for different modulation indices. Due to the space vector symmetry, the variation for only one sector is depicted in Fig. 5.

The variation of the  $I_{cap(rms)}$  with the modulation indices is also depicted in Fig. 6. The line current is assumed to be constant at rated value and the displacement power factor is taken to be one. The variation of the modulation index, changes the fundamental component of the output voltage and thus the  $V_D$  also varies linearly with the  $M$ . This changes the power processed by the VSC and thus the stress on dc-link capacitor also varies. The proposed analytical method considers the effect of the line current ripple and thus the accuracy improves substantially. The effect of the PWM scheme on  $I_{cap(rms)}$  is also studied and the variation of  $I_{cap(rms)}$  with  $M$  for the SVM and the DPWM1 is depicted in Fig. 6. The switching frequency is taken to be the same in both cases although the number of commutations is different. It is apparent from Fig. 6 that the use of the SVM would result in lower dc-link stress compared to the DPWM1. This is because the SVM has a smaller line current ripple compared to the

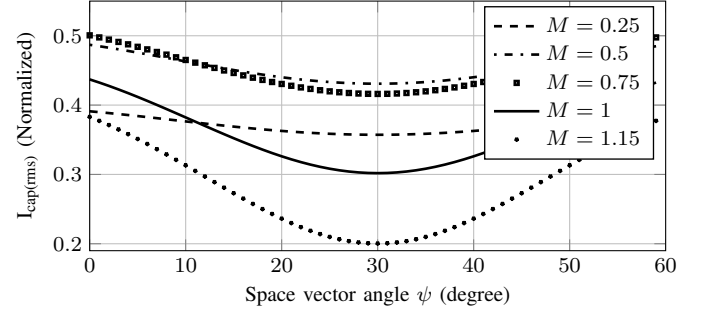


Fig. 5. The variation of the rms value of the dc-link capacitor current (normalized) with the reference space vector angle  $\psi$  for different values of the modulation indices for the SVM. The line current is kept constant at the rated value and the displacement power factor ( $\cos \phi$ ) is taken to be 1. The pulse ratio  $f_{sw}/f_0$  is 51.

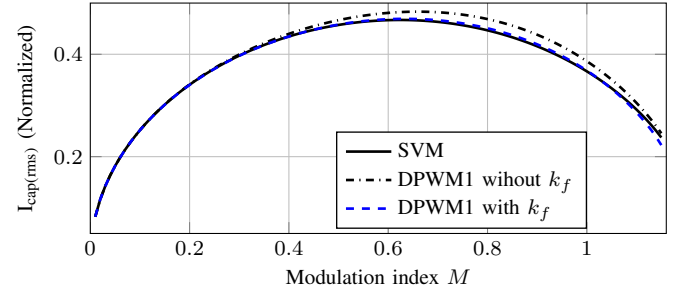


Fig. 6. The variation of the rms value of the dc-link capacitor current (normalized) with the modulation index  $M$ .

DPWM1. For fair comparison between the continuous and discontinuous PWM, the switching frequency of the DPWM1 is increased by multiplying the a switching frequency of the SVM to the frequency correction factor  $k_f = 3/2$  [6] and the result is also depicted in Fig. 6.

##### B. The Effect of the Displacement Power Factor Angle

The variation of the  $I_{cap(rms)}$  with the space vector angle  $\psi$  for different displacement power factor angle is depicted in Fig. 7 for the modulation index of  $M = 1$ . The strong space dependency of the  $I_{cap(rms)}$  for different power factor is evident from Fig. 7. For higher modulation indices, the dwell time of the voltage vector  $\vec{V}_1$  is dominant for space vector angle  $\psi < 30^\circ$ . The VSC input current  $I$  is equal to the line current of phase A, when  $\vec{V}_1$  is applied and thus the magnitude of  $I_a$  has a strong influence on  $I_{cap(rms)}$  in the first sub sector of the space vector diagram ( $0^\circ \leq \psi < 30^\circ$ ). For unity power factor, the line current of phase A is near it's peak value in this region. With the increase in the  $\psi$ , the magnitude of  $I_a$  also decreases and thus the reduction in  $I_{cap(rms)}$  is also observed in sub sector 1 ( $0^\circ \leq \psi < 30^\circ$ ). Similarly the magnitude of line current of phase C, strongly influences the  $I_{cap(rms)}$  in sub sector 2 ( $30^\circ \leq \psi < 60^\circ$ ), because the dwell time of  $\vec{V}_2$  is dominant in this region. For unity power factor operation, the magnitude of  $I_c$  increases with increase in  $\psi$  and reaches it's peak value at the end of the sub sector 2 and similar behavior of  $I_{cap(rms)}$  is also observed in sub sector 2.

TABLE I  
DC-LINK CAPACITOR CURRENT DESCRIPTION IN A HALF SWITCHING CYCLE FOR DIFFERENT SWITCHING SEQUENCES

Sequence	Time interval	DC-link capacitor current $I_{cap}(t)$
7210	$0_+ \leq t \leq (\frac{T_z}{4})_-$	$I_{cap}(t) = -I_{dc}$
	$(\frac{T_z}{4})_+ \leq t \leq (\frac{T_z}{4} + \frac{T_2}{2})_-$	$I_{cap}(t) = \left[ (I_Q \sin(\psi + 120^\circ) - I_D \cos(\psi + 120^\circ)) - \frac{V_{dc}T_z}{6L_f} - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 + \frac{3}{4}M \cos(\psi + 120^\circ) \right) t$
	$(\frac{T_z}{4} + \frac{T_2}{2})_+ \leq t \leq (\frac{T_z}{4} + \frac{T_2}{2} + \frac{T_1}{2})_-$	$I_{cap}(t) = \left[ (I_D \cos \psi - I_Q \sin \psi) - \frac{V_{dc}(T_z + T_2)}{6L_f} - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 - \frac{3}{4}M \cos \psi \right) t$
	$(\frac{T_z}{4} + \frac{T_2}{2} + \frac{T_1}{2})_+ \leq t \leq (\frac{T_s}{2})_-$	$I_{cap}(t) = -I_{dc}$
127	$0_+ \leq t \leq (\frac{T_1}{2})_-$	$I_{cap}(t) = \left[ (I_D \cos \psi - I_Q \sin \psi) - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 - \frac{3}{4}M \cos \psi \right) t$
	$(\frac{T_1}{2})_+ \leq t \leq (\frac{T_1 + T_2}{2})_-$	$I_{cap}(t) = \left[ (I_Q \sin(\psi + 120^\circ) - I_D \cos(\psi + 120^\circ)) - \frac{V_{dc}T_1}{6L_f} - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 + \frac{3}{4}M \cos(\psi + 120^\circ) \right) t$
	$(\frac{T_1 + T_2}{2})_+ \leq t \leq (\frac{T_s}{2})_-$	$I_{cap}(t) = -I_{dc}$
721	$0_+ \leq t \leq (\frac{T_s}{2})_-$	$I_{cap}(t) = -I_{dc}$
	$(\frac{T_s}{2})_+ \leq t \leq (\frac{T_s + T_2}{2})_-$	$I_{cap}(t) = \left[ (I_Q \sin(\psi + 120^\circ) - I_D \cos(\psi + 120^\circ)) - \frac{V_{dc}T_s}{3L_f} - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 + \frac{3}{4}M \cos(\psi + 120^\circ) \right) t$
	$(\frac{T_s + T_2}{2})_+ \leq t \leq (\frac{T_s}{2})_-$	$I_{cap}(t) = \left[ (I_D \cos \psi - I_Q \sin \psi) - \frac{V_{dc}(T_s + \frac{T_2}{2})}{3L_f} - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 - \frac{3}{4}M \cos \psi \right) t$
012	$0_+ \leq t \leq (\frac{T_s}{2})_-$	$I_{cap}(t) = -I_{dc}$
	$(\frac{T_s}{2})_+ \leq t \leq (\frac{T_s + T_1}{2})_-$	$I_{cap}(t) = \left[ (I_D \cos \psi - I_Q \sin \psi) - \frac{V_{dc}T_s}{3L_f} - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 - \frac{3}{4}M \cos \psi \right) t$
	$(\frac{T_s + T_1}{2})_+ \leq t \leq (\frac{T_s}{2})_-$	$I_{cap}(t) = \left[ (I_Q \sin(\psi + 120^\circ) - I_D \cos(\psi + 120^\circ)) - \frac{V_{dc}(T_s + \frac{T_1}{2})}{3L_f} - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 + \frac{3}{4}M \cos(\psi + 120^\circ) \right) t$
210	$0_+ \leq t \leq (\frac{T_2}{2})_-$	$I_{cap}(t) = \left[ (I_Q \sin(\psi + 120^\circ) - I_D \cos(\psi + 120^\circ)) - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 + \frac{3}{4}M \cos(\psi + 120^\circ) \right) t$
	$(\frac{T_2}{2})_+ \leq t \leq (\frac{T_1 + T_2}{2})_-$	$I_{cap}(t) = \left[ (I_D \cos \psi - I_Q \sin \psi) - \frac{V_{dc}T_2}{6L_f} - I_{dc} \right] + \frac{2V_{dc}}{3L_f} \left( 1 - \frac{3}{4}M \cos \psi \right) t$
	$(\frac{T_1 + T_2}{2})_+ \leq t \leq (\frac{T_s}{2})_-$	$I_{cap}(t) = -I_{dc}$

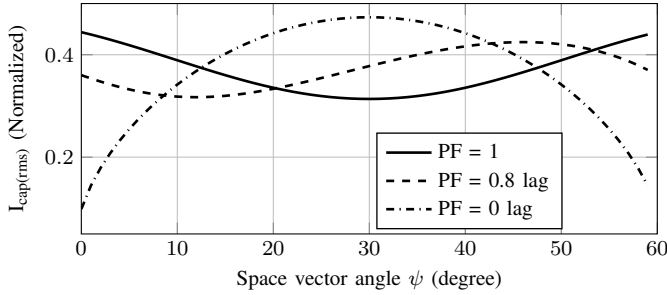


Fig. 7. The variation of the rms value of the dc-link capacitor current (normalized) as a function of space vector angle  $\psi$  for different displacement power factor ( $\cos \phi$ ) for the modulation index  $M=1$ .

For applications where the VSC is required to supply only the reactive power, the magnitude of  $I_a$  is close to zero in the vicinity of  $\psi = 0$ . In this region, the dwell time of the voltage vector  $\vec{V}_1$  dominates and thus the  $I_{cap(rms)}$  is also lowest in this region. The similar behavior is observed in the sub sector 2 for zero displacement power factor as it is evident from Fig. 7. The space dependency of  $I_{cap(rms)}$  for 0.8 (lagging) power factor is also shown in Fig. 7.

The  $I_{cap(rms)}$  as a function of displacement power factor angle for grid connected applications is shown in Fig. 8. The cases with different modulation indices are depicted. The line

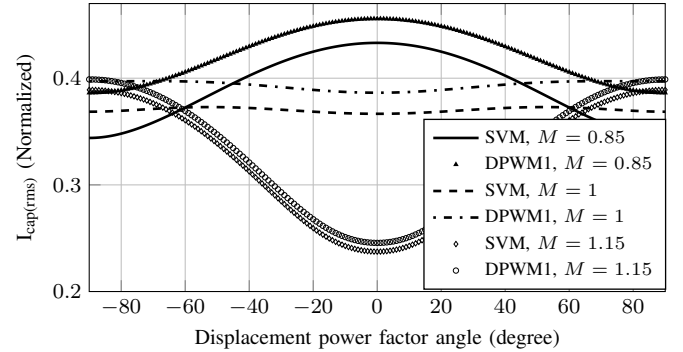


Fig. 8. The rms value of  $I_{cap}$  as a function of displacement power factor angle  $\phi$  for different modulation indices with line current maintained constant at the rated value.

current is assumed to be maintained constant at the rated value and the active and reactive components are varied. For the grid connected applications, where the VSC is mainly required to process the active power, the power factor is maintained close to one for most of the time. In such applications, operation at the higher modulation indices is desirable to reduce the stress on the dc-link capacitor. With the increase in the modulation index, the dwell time of the zero vector reduces. The dc-link capacitor sinks the source current  $I_{dc}$  during this interval and



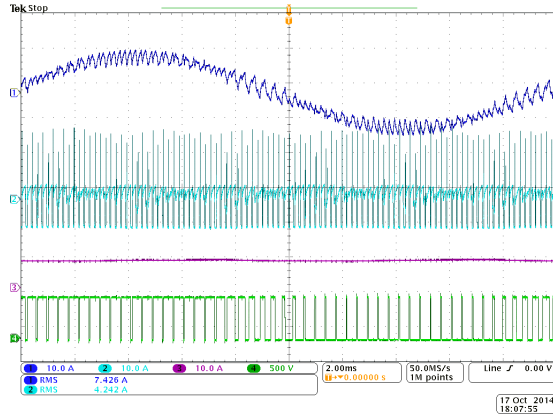


Fig. 9. Various waveforms for the unity power operation at  $M = 1$ . Ch1: Line current of phase A  $I_A$ , Ch2: Capacitor current  $I_{cap}$ , Ch3: Input current  $I_{dc}$ , Ch4: Pole voltage of phase A.

the reduction in  $T_z$  leads to reduced  $I_{cap(rms)}$ . This is also shown in Fig. 8, where the  $I_{cap(rms)}$  decreases with increase in the modulation index for unity power factor operation. For static Var compensation applications, where the VSC primarily supplies the reactive power, the lower modulation index results in smaller  $I_{cap(rms)}$ . However, the reduction in  $I_{cap(rms)}$  is marginal and dc-link voltage should be chosen based on the other performance attributes.

## V. EXPERIMENTAL RESULTS

To verify the analysis, set of experiments have been carried out on a laboratory scale prototype of 5 kVA. The switching frequency is taken to be 2.55 kHz. The dc-link voltage is set to 600 V and the line filter inductor is taken to be 3 mH. The VSC is connected to the programmable ac load. The programmable ac load is operated in the constant current mode to maintain the fundamental frequency component of the line current constant. The relevant waveforms for the SVM at the unity power factor at  $M = 1$  is shown in Fig. 9. The rms value of the capacitor current is obtained for the different modulation indices for the SVM and the DPWM1 for the unity power factor load. The carrier frequency is taken to be the same for both of the PWM schemes. The rms values of the capacitor current are normalized to the peak value of the fundamental component of the line current (10.24 A) and shown in Fig. 10. The experimental results shown in the Fig. 10 closely matches with the analytical results shown in Fig. 6.

## VI. CONCLUSION

An analytical method to calculate the rms value of the dc-link current in the VSC is presented. The influence of the line current ripple on the rms value of the dc-link current is considered, which yields accurate analytical results. Each PWM scheme have different line current ripple and the proposed analytical method can be effectively used to evaluate the effect of the PWM scheme on the dc-link current stress. The SVM and the DPWM1 schemes are compared. It is observed that the use of the SVM results in lower dc-link current stress. The

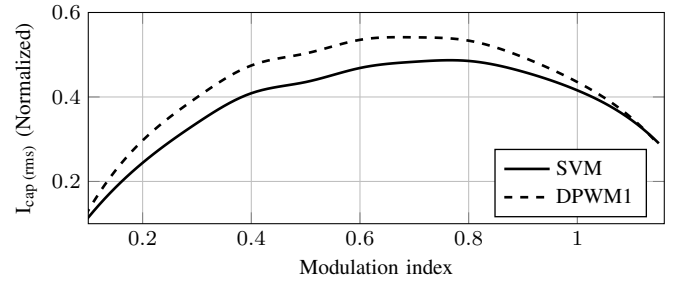


Fig. 10. The variation of the measured rms value of the dc-link capacitor current (normalized) with the modulation index  $M$  for the SVM and the DPWM1.

displacement power factor has a strong influence on the rms value of the dc-link current. For grid connected applications, where the power factor is close to unity, operation with higher modulation indices is desirable to reduce the stress on dc-link. The proposed analytical method is also verified experimentally and good agreement between the analysis and the experimental results is observed.

## REFERENCES

- [1] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters - an overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sept 2014.
- [2] J. Kolar and S. Round, "Analytical calculation of the rms current stress on the dc-link capacitor of voltage-pwm converter systems," *IEE Proc. Electric Power Applications*, vol. 153, no. 4, pp. 535–543, July 2006.
- [3] M. Vogelsberger, T. Wiesinger, and H. Ertl, "Life-cycle monitoring and voltage-managing unit for dc-link electrolytic capacitors in pwm converters," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 493–503, Feb 2011.
- [4] Y. Yu, T. Zhou, M. Zhu, and D. Xu, "Fault diagnosis and life prediction of dc-link aluminum electrolytic capacitors used in three-phase ac/dc/ac converters," in *Proc. Second International Conference on Instrumentation, Measurement, Computer, Communication and Control (IMCCC)*, 2012, Dec 2012, pp. 825–830.
- [5] P. Dahono, Y. Sato, and T. Kataoka, "Analysis and minimization of ripple components of input current and voltage of pwm inverters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 4, pp. 945–950, Jul 1996.
- [6] A. Hava, R. Kerkman, and T. Lipo, "Simple analytical and graphical methods for carrier-based pwm-vsi drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan 1999.
- [7] B. McGrath and D. Holmes, "A general analytical method for calculating inverter dc-link current harmonics," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1851–1859, Sept 2009.
- [8] M. Bierhoff and F. Fuchs, "Dc-link harmonics of three-phase voltage-source converters influenced by the pulsewidth-modulation strategy - an analysis," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 2085–2092, May 2008.
- [9] P. Evans and R. Hill-Cottingham, "Dc link current in pwm inverters," *Proc. Electric Power Applications*, vol. 133, no. 4, pp. 217–224, July 1986.
- [10] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ: Wiley-IEEE Press, 2003.
- [11] G. Narayanan and V. T. Ranganathan, "Analytical evaluation of harmonic distortion in pwm ac drives using the notion of stator flux ripple," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 466–474, 2005.
- [12] G. Narayanan, H. Krishnamurthy, D. Zhao, and R. Ayyanar, "Advanced bus-clamping pwm techniques based on space vector approach," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 974–984, 2006.
- [13] G. Narayanan, V. T. Ranganathan, D. Zhao, H. Krishnamurthy, and R. Ayyanar, "Space vector based hybrid pwm techniques for reduced current ripple," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1614–1627, 2008.